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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of Atty. Docket No.

MARCEL E.I. BROEKAART ET AL NL 000314

Serial No. 09/804,004 Group Art Unit: 2812

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A METHOD OF MANUFACTURING A SEMICONDUCTOR DEVICE

Honorable Commissioner of Patent and Trademarks
Washington, D.C. 20231

CLAIM FOR PRIORITY

Sir:

A certified copy of the European Application No. 00201928.9 filed May 31, 2000 referred to in the Declaration of the above-identified application is attached herewith.

Applicants claim the benefit of the filing date of said European application.

Respectfully submitted,

By _____
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Enclosure

CERTIFICATE OF MAILING

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Bescheinigung | Certificate | Attestation

Die angehefteten Unterlagen stimmen mit der ursprünglich eingereichten Fassung der auf dem nächsten Blatt bezeichneten europäischen Patentanmeldung überein.

The attached documents are exact copies of the European patent application described on the following page, as originally filed.

Les documents fixés à cette attestation sont conformes à la version initialement déposée de la demande de brevet européen spécifiée à la page suivante.

Patentanmeldung Nr. | Patent application No. | Demande de brevet n°

00201928.9

Der Präsident des Europäischen Patentamts;
Im Auftrag

For the President of the European Patent Office

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Blatt 2 d r Bescheinigung
Sheet 2 of the certificate
Page 2 de l'attestation

Anmeldung Nr.:
Application no.:
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Date of filing:
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Anmelder:
Applicant(s):
Demandeur(s):
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NETHERLANDS

Bezeichnung der Erfindung:
Title of the invention:
Titre de l'invention:
A method of manufacturing a semiconductor device

In Anspruch genommene Priorität(en) / Priority(ies) claimed / Priorité(s) revendiquée(s)

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Contracting states designated at date of filing: AT/BE/CH/CY/DE/DK/ES/FI/FR/GB/GR/IE/IT/LI/LU/MC/NL/PT/SE/[redacted]
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Bemerkungen:
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Remarques:

A method of manufacturing a semiconductor device

The invention relates to a method of manufacturing an electronic device, a semiconductor device in particular but not exclusively, which method comprises the steps of:

- applying a semiconductor substrate which is provided at a surface with a conductor, the conductor having a top surface portion and side wall portions, of which at least the top surface portion is provided with an etch stop layer,
- applying a dielectric layer,
- etching a via in the dielectric layer over the conductor, and stopping on the etch stop layer to create an exposed part of the etch stop layer,
- removing the exposed part of the etch stop layer within the via from at least the top surface portion of the conductor,
- filling the via with a conductive material.

Such a method is known from US-A-5,451,543, wherein a dielectric material, i.e. silicon nitride or aluminium oxide, or a conductive material, i.e. tungsten, titanium nitride or tantalum nitride, is used for the etch stop layer.

A disadvantage of the use of tungsten, titanium nitride or tantalum nitride for the etch stop layer is that metallic polymers are formed during etching of the via in the dielectric layer at the moment the etch chemistry applied interacts with the conductive material of the etch stop layer. The larger the difference in depths of the vias to be etched simultaneously in the dielectric layer, the more pronounced the above-mentioned metallic polymer formation takes place. Because these metallic polymers degrade the electrical via resistance, much effort has to be put in their removal, which is most efficiently done by etching using a wet chemistry. However, owing to their porous and otherwise unstable nature, most low-k materials appear to be incompatible with such wet etch chemistry, that is to say their low-k properties are degraded. A disadvantage of the use of silicon nitride or aluminium oxide for the etch stop layer is that both materials have a relatively high dielectric constant compared to silicon oxide or a low-k material, which adversely affects the parasitic capacitance of the semiconductor device.

The invention has *inter alia* for its object to provide a method of manufacturing a semiconductor device of the kind mentioned in the opening paragraph, which method counteracts the formation of metallic polymers when the etch stop layer is reached during via etching as well as reduces the parasitic capacitance of the resulting semiconductor device.

According to the invention, this object is achieved in that a layer comprising silicon carbide is applied as the etch stop layer. Silicon carbide has a smaller dielectric constant than silicon nitride en aluminium oxide and, hence, provides a semiconductor device with a reduced parasitic capacitance. Moreover, the formation of metallic polymers during via etching is less pronounced, as silicon carbide is attacked to a lesser degree by the etch chemistry applied than is tungsten, titanium nitride and tantalum nitride.

The conductor having a top surface portion and side wall portions, of which at least the top surface portion is provided with the etch stop layer, may be formed by depositing a stack of a conductive layer with on top thereof the etch stop layer, and subsequently patterning the stack. However, it is advantageous to form the conductor first by depositing a conductive layer and patterning it, and subsequently apply the etch stop layer to the top surface portion and the side wall portions of the conductor. In this way the conductor is encapsulated by the etch stop layer, which is advantageous during etching of a via which is unlanded, that is to say a via which potentially falls off the conductor instead of completely landing on the top surface portion of the conductor. The etch stop layer present at the side wall portions of the conductor counteracts interaction between the etch chemistry applied during etching of the unlanded via and the material of the conductor and, hence, counteracts formation of metallic polymers.

Further advantageous embodiments of the method in accordance with the invention are described in the dependent claims.

These and other aspects of the invention will be apparent from and be elucidated with reference to the embodiments described hereinafter and shown in the drawing. In the drawing:

Figs. 1 to 4 show in diagrammatic cross-sectional views successive stages in the manufacture of a semiconductor device using the method in accordance with the invention.

Fig. 1 shows a portion of a semiconductor device which serves as an appropriate starting point for describing the method in accordance with the invention. The semiconductor device comprises a semiconductor substrate 1 which is provided at a surface 2 with conductors 3,4,5, which conductors 3,4,5 each have a top surface portion 6 and side wall portions 7. It is noted that, although the invention is described in the context of three conductors and three vias, it is also applicable to just one conductor and one via. In reality, a semiconductor device will comprise a plurality of such conductors and vias. Although illustrated as one element, the semiconductor substrate 1 is actually likely to include multiple layers which are formed on, for example, a semiconductor body composed of, for example, silicon. For simplicity, the multiple layers together with the body, on which these layers are formed, are compositely illustrated as a single layer, namely semiconductor substrate 1. Functionally, the conductors 3,4,5 can be, for example, gates of a metal oxide semiconductor field effect transistor (MOSFET) or a thin film transistor (TFT), bases or emitters of a bipolar or BICMOS device, or can be part of, for example, a metal layer of a multi-level interconnect structure. The conductors 3,4,5 consist of a capping layer 8 on top of a base metal portion 11, the capping layer 8 thereby providing the top surface portion 6 of the conductors 3,4,5. The base metal portion 11 is comprised of aluminium in the present example. However, other materials such as, for example, copper or tungsten can be used as well. In the present example, a double-layer consisting of a titanium layer 9 with on top thereof a titanium nitride layer 10 is applied as the capping layer 8. It is noted that the capping layer 8, which is usually applied to act as an anti-reflective coating during patterning of the base metal portion 11, is an optional part of the conductors 3,4,5. Another suitable material such as titanium tungsten, tungsten nitride and tantalum nitride may also be used instead of titanium nitride. Alternatively, the capping layer 8 may consist of a single layer of, for example, titanium nitride, titanium tungsten, tungsten nitride or tantalum nitride. In that situation, the capping layer 8 is advantageously removed within the vias prior to filling the vias with conductive material, as high-resistant material may be formed due to interaction between the base metal portion 11 and the capping layer 8, which high-resistant material adversely affects the electrical via resistance.

The conductors 3,4,5 are formed in accordance with conventional processing. For example, a stack consisting of a layer of aluminium, a layer of titanium and a layer of titanium nitride is deposited on the surface 2 of the semiconductor substrate 1, which stack of layers is then patterned so as to form the conductors 3,4,5 of Fig. 1.

After formation of the conductors 3,4,5, an etch stop layer 12 is applied to the top surface portion 6 and the side wall portions 7 of the conductors 3,4,5 as well as to those portions of the semiconductor substrate 1 which are not covered by the conductors 3,4,5. In accordance with the invention, the etch stop layer 12 is composed of silicon carbide, which layer can be deposited by means of, for example, chemical vapor deposition (CVD). The thickness of the etch stop layer 12 may be, for example, in the range between about 10 nm and 100 nm. Alternatively, a stack consisting of a layer of aluminium, a layer of titanium, a layer of titanium nitride and a layer of silicon carbide may be deposited and subsequently patterned. In that case, the etch stop layer 12 of silicon carbide would only be present at the top surface portion 6 of the conductors 3,4,5, whereas the side wall portions 7 of the conductors 3,4,5 would not be covered by the etch stop layer 12.

After deposition of the etch stop layer 12 composed of silicon carbide, a dielectric layer 13 is deposited on the etch stop layer 12 (Fig. 2). The dielectric layer 13 may be composed of silicon oxide. However, it is advantageously composed of a material having a dielectric constant lower than that of silicon oxide such as, for example, hydrogen silsesquioxane, parylene, a fluorinated polyimide, or "SILK©" which is marketed by Dow Chemical from Midland, Michigan, USA. Such dielectric layer can be deposited by a conventional deposition technique such as, for example, spin-coating.

After deposition, the dielectric layer 13, which is composed of hydrogen silsesquioxane in the present example, is patterned so as to form vias 14,15,16 overlying the conductors 3,4,5. Patterning is accomplished using conventional photolithographic techniques, wherein a photoresist layer (not shown) is deposited on the dielectric layer 13, which photoresist layer is selectively exposed to radiation and developed in order to form a resist mask (not shown) having openings which expose the dielectric layer 13 at the areas of the vias 14,15,16 to be formed. Subsequently, the vias 14,15,16 are etched by removing the unmasked areas of the dielectric layer 13.

Etching of the vias 14,15,16 is continued until all of the dielectric layer 13 is removed from above the conductors 3,4,5 within the unmasked via areas. In case of differential thicknesses of the dielectric layer 13 which typically occur across the semiconductor device, certain vias may be exposed to the etch chemistry for a prolonged

period of time, such that an over-etch occurs. During such over-etch, metallic polymers may be formed due to interaction between the etch chemistry applied and the material of the conductors exposed within these vias. Moreover, if a via is slightly misaligned, which is the case for via 15 overlying conductor 4 (Fig. 2), the over-etch will result in formation of a trench 17 along at least one of the side wall portions 7 of the conductor 4. Such misaligned via, being also referred to as unlanded via, potentially falls off the conductor instead of completely landing on the top surface portion of the conductor. If the over-etch is severe in case of such unlanded via, the trench 17 may even reach the semiconductor substrate 1, which may be locally composed of conductive material as well. Attack of such semiconductor substrate 1 during via etching may also result in formation of metallic polymers. However, in order to counteract the above-mentioned problems, via etching is performed selectively to the etch stop layer 12 of silicon carbide, which etch stop layer 12 is present on the top surface portion 6 and the side wall portions 7 of the conductors 3,4,5 and the portions of the semiconductor substrate 1 not covered by the conductors 3,4,5. Hence, an over-etch does not expose the semiconductor substrate 1 nor any portions, whether top surface portions or side wall portions, of the conductors 3,4,5. Formation of metallic polymers through interaction between the etch chemistry used during via etching and the material of the conductors 3,4,5 or the semiconductor substrate 1 is thus counteracted.

To achieve the above-mentioned selectivity of via etching, an etch chemistry is used which etches the dielectric layer 13, in the present example composed hydrogen silsesquioxane, much faster than the etch stop layer 12 composed of silicon carbide. A suitable etch chemistry which may be used to form vias 14,15,16 while stopping on the etch stop layer 12 is, for example, a fluorine carbon dry etch chemistry. In this way, the etch stop layer 12 of silicon carbide is exposed within the vias 14,15,16.

In order to make contact to the conductors 3,4,5, the exposed parts of the etch stop layer 12 of silicon carbide need to be removed within the vias 14,15,16 (Fig. 3). The etch stop layer 12 exposed within the vias 14,15,16 can be removed from the top surface portion 6 of the conductors 3,4,5 as well as from the at least one of the side wall portions 7 of the conductor 4, over which the unlanded via 15 lies. However, the etch stop layer 12 of silicon carbide is advantageously removed from only the top surface portion 6 of the conductors 3,4,5, which removal is advantageously carried out anisotropically using, for example, a fluorine carbon dry etch chemistry. As illustrated in Fig. 3, an anisotropic etch removes the exposed parts of the etch stop layer 12 from the top surface portion 6 of the conductors 3,4,5, while only recessing the exposed parts of the etch stop layer 12 along the at

least one of the side wall portions 7 of the conductor 4. As the thickness of the etch stop layer 12 of silicon carbide, which may be somewhere between about 10 nm and 100 nm, is relatively small and relatively uniform across the semiconductor device, it can be removed in a very controlled way without causing severe interaction between the etch chemistry applied and the material of the conductors 3,4,5 and, hence, without causing severe formation of metallic polymers.

In the present example, the capping layer 8, which consists of a titanium layer 9 with on top thereof a titanium nitride layer 10, is left in place within the vias 14,15,16 after removal of the etch stop layer 12 from the top surface portion 6 of the conductors 3,4,5. However, in case the capping layer 8 consists of a single layer of, for example, titanium nitride, titanium tungsten, tungsten nitride or tantalum nitride, it is advantageously removed within the vias 14,15,16 prior to filling the vias 14,15,16 with conductive material, as high-resistant material may be formed due to interaction between the base metal portion 11 and the capping layer 8, which high-resistant material adversely affects the electrical via resistance.

In a next step (Fig. 4), the vias 14,15,16 are filled with a conductive material 18 by means of, for example, deposition of a layer of, for example, aluminium, copper or tungsten. It is noted that the layer of conductive material is advantageously applied as a double-layer consisting of a layer comprising the metal such as, for example, aluminium, copper or tungsten, on top of a layer acting as adhesion layer and/or barrier layer. In this respect titanium may be applied as adhesion layer and titanium nitride or titanium tungsten as barrier layer. The deposited layer of conductive material may subsequently be etched while using an oversized mask. In the present example, however, the deposited layer of conductive material is maskless removed until the dielectric layer 13 is exposed, as is shown in Fig. 4. Maskless removal of the layer of conductive material can be accomplished by means of, for example, chemical-mechanical polishing (CMP) e.g. using a commercially available slurry.

It will be apparent that the invention is not limited to the embodiments described above, but that many variations are possible to those skilled in the art within the scope of the invention.

CLAIMS:

1. A method of manufacturing an electronic device, a semiconductor device in particular but not exclusively, which method comprises the steps of:
- applying a semiconductor substrate (1) which is provided at a surface (2) with a conductor (3,4,5), the conductor (3,4,5) having a top surface portion (6) and side wall portions (7), of which at least the top surface portion (6) is provided with an etch stop layer (12),
- applying a dielectric layer (13),
- etching a via (14,15,16) in the dielectric layer (13) over the conductor (3,4,5), and stopping on the etch stop layer (12) to create an exposed part of the etch stop layer (12),
- removing the exposed part of the etch stop layer (12) within the via (14,15,16) from at least the top surface portion (6) of the conductor (3,4,5),
- filling the via (14,15,16) with a conductive material (18)
characterized in that a layer comprising silicon carbide is applied as the etch stop layer (12).

2. A method as claimed in claim 1, characterized in that the etch stop layer is applied to the top surface portion and the side wall portions of the conductor after the provision of the conductor at the surface of the semiconductor substrate.

3. A method as claimed in claim 2, characterized in that the via is etched while overhanging at least one of the side wall portions of the conductor and exposing at least part of the etch stop layer, which etch stop layer covers the top surface portion and the at least one of the side wall portions of the conductor.

4. A method as claimed in claim 3, characterized in that the etch stop layer is removed within the via from only the top surface portion of the conductor.

5. A method as claimed in claim 2, 3 or 4, characterized in that the etch stop layer is applied to the top surface portion and the side wall portions of the conductor as well as to portions of the semiconductor substrate which are not covered by the conductor.

6. A method as claimed in any one of the preceding claims, characterized in that the conductor is provided while being comprised at least in part of a material selected from a group comprising aluminium, copper and tungsten.

7. A method as claimed in any one of the preceding claims, characterized in that the conductor is provided while comprising a capping layer, which capping layer provides the top surface portion of the conductor.

8. A method as claimed in claim 7, characterized in that the capping layer is comprised of a material selected from a group comprising titanium nitride, titanium tungsten and tantalum nitride.

9. A method as claimed in any one of the preceding claims, characterized in that the dielectric layer is applied by depositing a dielectric material having a dielectric constant lower than that of silicon oxide.

10. A method as claimed in claim 9, characterized in that the dielectric layer is applied by depositing a material selected from a group comprising hydrogen silsesquioxane, parylene and a fluorinated polyimide.

11. A method as claimed in any one of the preceding claims, characterized in that the via is filled by depositing a conductive layer, which conductive layer comprises a metal selected from a group comprising aluminium, copper and tungsten.

ABSTRACT:

A method of manufacturing an electronic device, a semiconductor device in particular but not exclusively, which method comprises the steps of:

- applying a semiconductor substrate (1) which is provided at a surface (2) with a conductor (3,4,5), the conductor (3,4,5) having a top surface portion (6) and side wall portions (7), of which at least the top surface portion (6) is provided with an etch stop layer (12) comprising silicon carbide,
- applying a dielectric layer (13),
- etching a via (14,15,16) in the dielectric layer (13) over the conductor (3,4,5), and stopping on the etch stop layer (12) to create an exposed part of the etch stop layer (12),
- removing the exposed part of the etch stop layer (12) within the via (14,15,16) from at least the top surface portion (6) of the conductor (3,4,5),
- filling the via (14,15,16) with a conductive material (18).

Fig. 4

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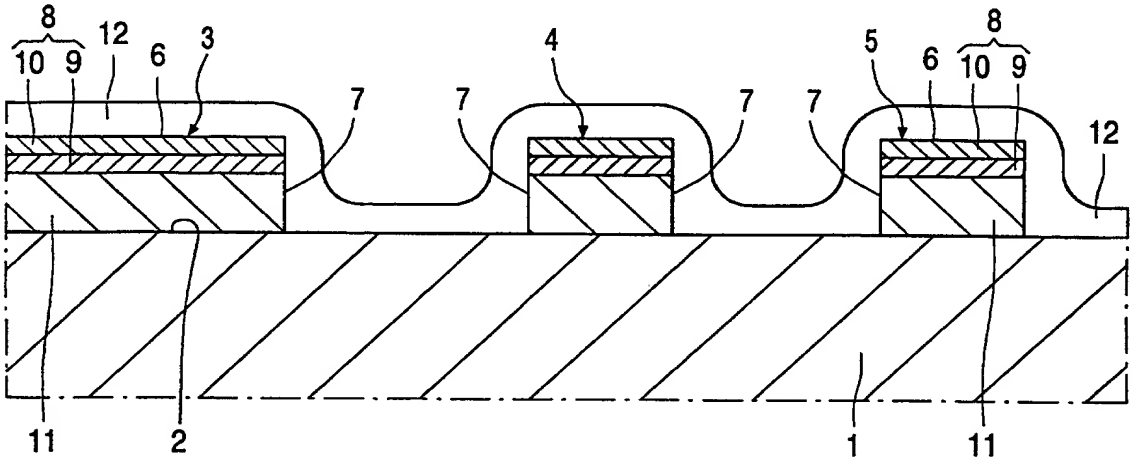

FIG. 1

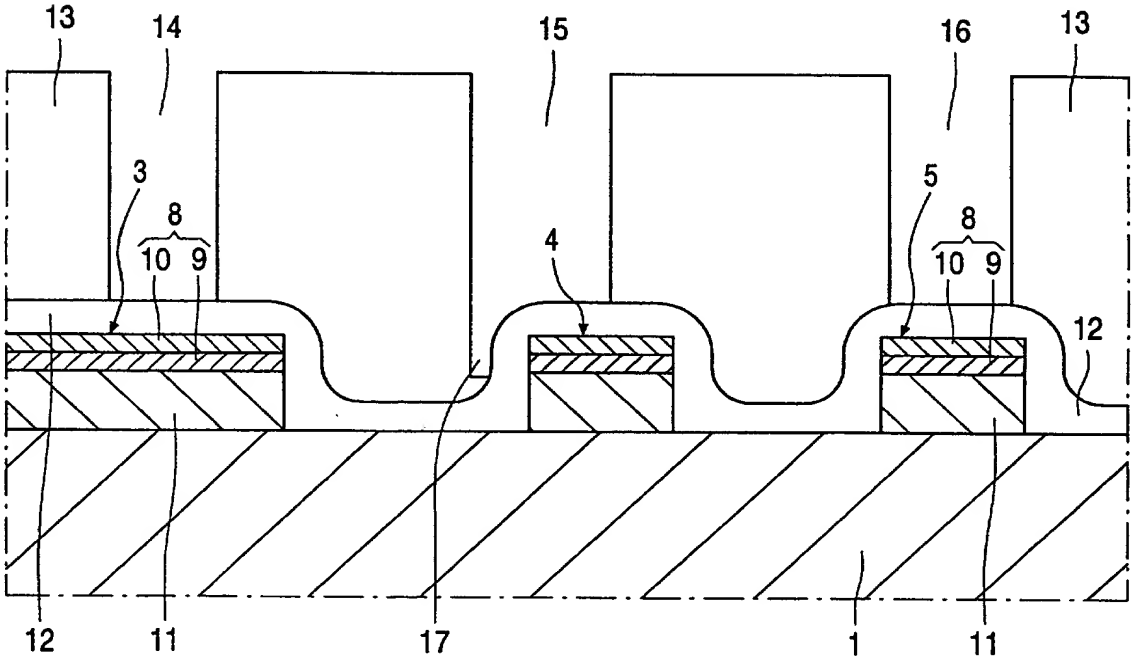

FIG. 2

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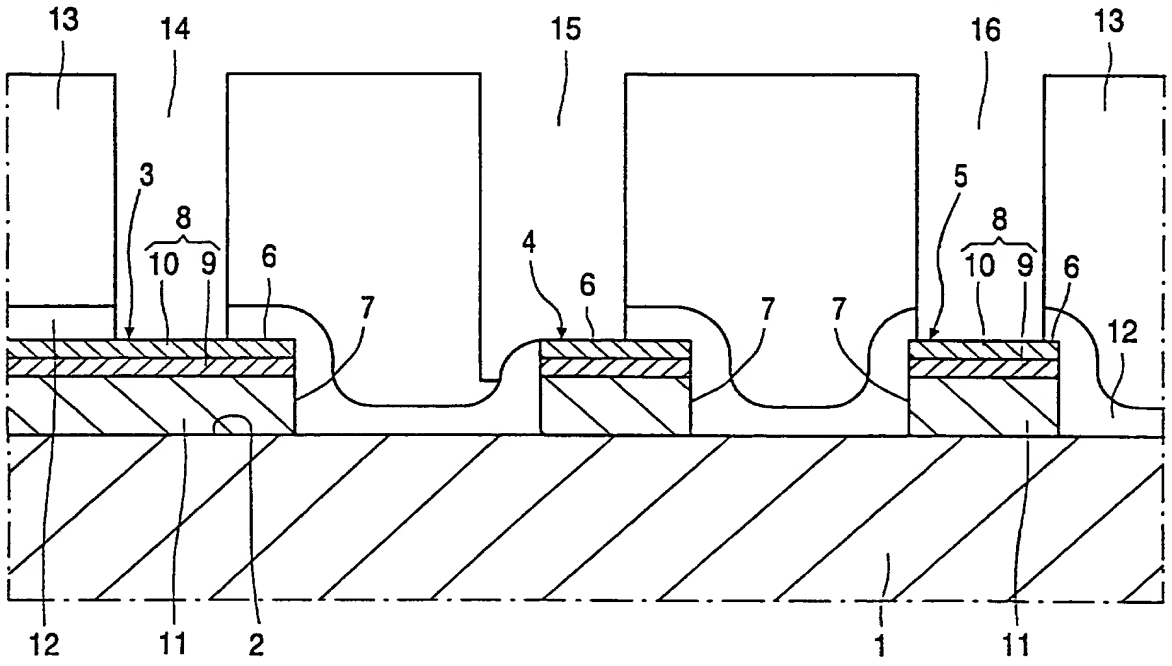
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FIG. 3

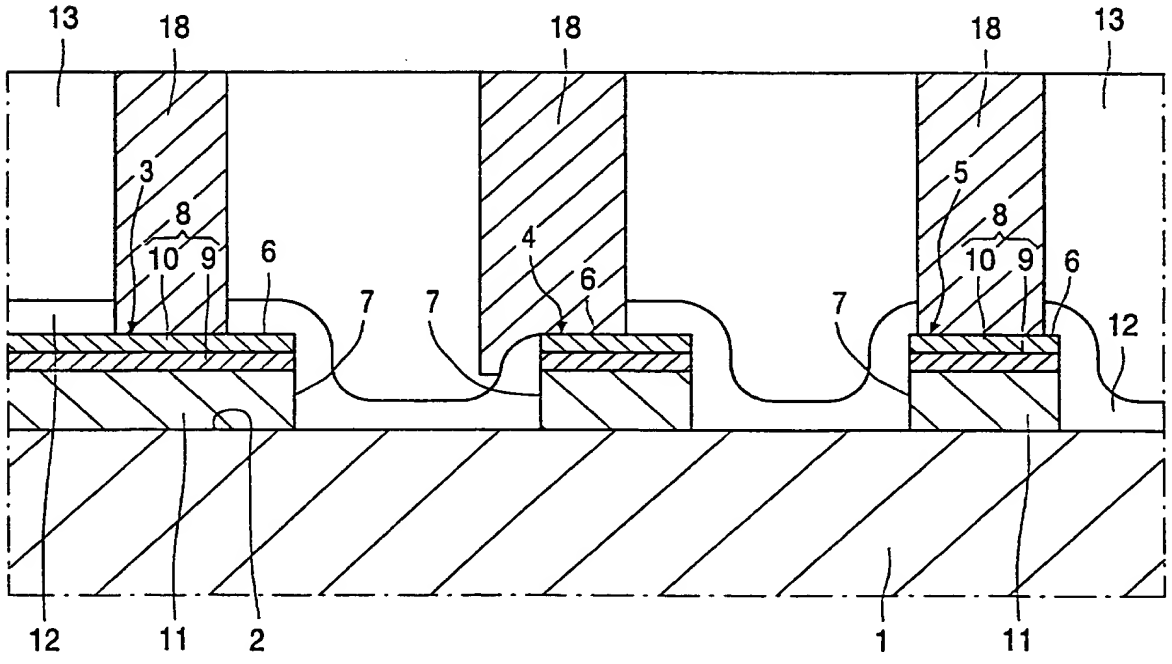
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FIG. 4